Attorney Docket No. 042390.P5346

Patent

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Patent Application of	Examiner: Verbrugge, K.
Thomas J. Holman	Art Unit: 2751
Serial No. 09/023,170	
Filed: February 13, 1998	
For: MEMORY SYSTEM INCLUDING A MEMORY MODULE HAVING A MEMORY MODULE CONTROLLER INTERFACING BETWEEN A SYSTEM MEMORY CONTROLLER AND MEMORY DEVICES OF THE MEMORY MODULE (As Amended)	

HONORABLE COMMISSIONER OF
PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPEAL BRIEF
(Under 37 C.F.R. §1.192)

Sir:

This is an appeal to the Board of Patent Appeals and Interferences from the decision of the Examiner of Group 2751, dated August 8, 2000, who finally rejected claims 1-20 in the above-identified application. This Appeal Brief is filed under 37 C.F.R. § 1.192. This Appeal Brief is submitted in triplicate pursuant to 37 C.F.R. § 1.192(a).

I. REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California, 95052.

II. RELATED APPEALS AND INTERFERENCES

Appellant identifies the following related applications, which may directly affect, be directly affected by, or have a bearing on the Board's decisions in connection with the present application.

The present application is related to and claims the benefit of U.S. Provisional Application No. 60/067,824, entitled "DISTRIBUTED CONTROL MEMORY BUS ARCHITECTURE," filed on December 5, 1997 and U.S. Provisional Application No. 60/067,588, entitled "DISTRIBUTED CONTROL MEMORY BUS ARCHITECTURE," also filed on December 5, 1997.

The above-identified application is also related to co-pending U.S. Patent Application No. 09/023,234 ('234 Application), entitled "MEMORY MODULE INCLUDING A MEMORY MODULE CONTROLLER,"[1] filed on February 13, 1998 and U.S. Patent Application No. 09/023,172 ('172 Application), entitled "MEMORY MODULE CONTROLLER,"[2] filed on February 13, 1998. A Notice of Appeal was filed on September 27, 2000 for the '234 Application and on September 27, 2000 for the '172 Application.

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[1] The title of the '172 Application has been amended to "MEMORY MODULE HAVING A MEMORY MODULE CONTROLLER CONTROLLING MEMORY TRANSACTIONS FOR A PLURALITY OF MEMORY DEVICES."

[2] The title of the '234 Application has been amended to "MEMORY MODULE CONTROLLER FOR PROVIDING AN INTERFACE BETWEEN A SYSTEM MEMORY CONTROLLER AND A PLURALITY OF MEMORY DEVICES ON A MEMORY MODULE."

The aforementioned provisional and co-pending applications are assigned to the same assignee of the present application on appeal.

III. STATUS OF THE CLAIMS

Claims 1-20 are finally rejected. Claims 1-20 are the subject of this appeal.

Claims 1-6, 8, 9, 13, and 15-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,045,781 to Levy et al. ("Levy").

Claims 7, 10, 11, 12, and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Levy.

Claims 1-20 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of co-pending Application No. 09/023,172 ('172 Application) and claims 1-17 of copending Application No. 09/023,234 ('234 Application).

A copy of claims 1-20 as they stand on appeal are set forth in the attached Appendix.

IV. STATUS OF AMENDMENTS

The present application was filed on February 13, 1998 with claims 1 through 20.

In the Office Action mailed February 9, 1999, the Examiner rejected claims 1-20 under 35 U.S.C. § 103(a) as being unpatentable over "Memory Systems Design and Applications," edited by Dave Bursky, pp. 213-220 (Bursky Reference) and rejected claims 1-20 under a 35 U.S.C. § 101 double patenting rejection as conflicting with claims 1-14 of the '172 Application and claims 1-17 of the '234 Application.

In response to the February 9, 1999 Office Action, Appellant filed a Continued Prosecution Application on August 9, 1999.

In the Office Action mailed on September 3, 1999, the Examiner provided new grounds of rejection in which claims 1-6, 9, 13, and 15-20 were rejected under 35 U.S.C. 102(b) as being anticipated by the Bursky Reference and claims 7, 8, 10-12, and 14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Bursky Reference. The Examiner also provisionally rejected claims 1-20 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 for the '172 Application and claims 1-17 of the '234 Application.

In response to the September 9, 1999 Office Action, Appellant filed an amendment on March 2, 2000. In the March 2, 2000 amendment, Appellant amended claims 1-10 and 15-18 and requested allowance of claims 1-20 over the Bursky Reference. Appellant also stated that upon a condition of allowance of one or more claims, Appellant will submit a timely terminal disclaimer to overcome the provisional double patenting rejection of claims 1-20 of the present application.

In the Office Action mailed on May 17, 2000, the Examiner asserted that Appellant's response filed on March 2, 2000 was not fully responsive to the Office Action mailed on September 9, 2000.

In response to the May 17, 2000 Office Action, Appellant filed a Response on May 25, 2000. In the May 25, 2000 Response, Appellant requested reconsideration of the present application in view of the remarks contained therein.

In the Office Action mailed on August 8, 2000, the Examiner provided a Final Rejection based on newly cited prior art. More particularly, the Examiner rejected claims 1-6, 8, 9, 13, and 15-20 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,045,781 to Levy *et al.* ("Levy") and claims 7, 10, 11, 12, and 14 under 35 U.S.C. § 103(a) as being unpatentable over Levy. The Examiner also maintained the previous

provisional double-patenting rejection of claims 1-20 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 for the '172 Application and claims 1-17 of the '234 Application.

In response to the August 8, 2000 Final Office Action, Appellant filed an Amendment After Final on September 27, 2000. In the September 27, 2000 Amendment After Final, Appellant amended claims 1, 4, 7, 9-10, and 15-17[1] and requested allowance of claims 1-20 over Levy. Appellant again stated that upon a condition of allowance of one or more claims, Appellant will submit a timely terminal disclaimer to overcome the provisional double patenting rejection of claims 1-20 of the present application.

In the Advisory Action mailed on October 19, 2000, the Examiner stated that the proposed amendments contained in the September 27, 2000 After Final Amendment will be entered upon filing a Notice of Appeal and an Appeal Brief.

In response to the October 19, 2000 Advisory Action, Appellant filed the Notice of Appeal on October 23, 2000 and this subsequent Appeal Brief. Accordingly, the amendments in the September 27, 2000 After Final Amendment are entered for purposes of appeal.

V. SUMMARY OF THE INVENTION

The present invention is defined by claims 1-20 and their equivalents. This section of the Appeal Brief is set forth merely to comply with the requirements of 37 C.F.R. § 1.192(c)(5) and is not intended to limit claim 1 or its equivalents in any way. *See* M.P.E.P. 1206.

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[1] In the September 27, 2000 After Final Amendment, claim 8 is inadvertently indicated as being ("Twice Amended"), however, no amendment was made to claim 8.

Claim 1 describes a system having a system memory controller and a first memory module. The first memory module includes a plurality of memory devices and a first memory module controller coupled to the system memory controller and the first plurality of memory devices. The first memory module controller is to receive from the system memory controller a first memory transaction in a first format and to convert the first memory transaction into a second memory transaction in a second format for the first plurality of memory devices. The second format of the second memory transaction is different from the first format of the first memory transaction.

The specification and drawings set forth embodiments of the invention, as defined, e.g., in claim 1. **FIG. 3** shows memory module controllers 310 and 316 coupled with a system memory controller 304 via system memory bus 323. Memory module controller 310 is coupled to a plurality of memory devices 312 through 315 via local memory module busses 330, 332, and 334-337. Memory module controller 316 is coupled to a plurality of memory devices 317-320 via local memory module busses 338, 340, and 341-344. (Spec. pp. 10-12). Memory module controllers 310 operate as bridges between system memory bus 323, that operates in one protocol or format, and local or memory module busses (e.g., lines 330, 332, and 334-337) that operate in a second different protocol format. (Spec. p.12, lines 19-22).

Thus, memory module controllers 310 and 316 for each memory module is an interface between system memory controller 304 and individual memory devices (e.g., memory devices 312-315 and 316-320) on the modules 306 and 308. Such an architecture allows for decoupling of individual memory devices form the system memory bus 323 and

the system memory controller 304. This allows for the independent development of the memory device technology. For example, the memory devices may be developed to be faster, wider, to operate at different operating supply voltages, or to operate with reduced voltage swings than if the memory devices where directly communicating with the system memory controller. (Spec. p. 9, lines 14-23).

VI. ISSUES

I. Whether claims 1-6, 8, 9, 13, and 15-20 are anticipated by Levy under 35 U.S.C. § 102(b).

II. Whether claims 7, 10, 11, 12, and 14 are unpatentable under 35 U.S.C. § 103(a) over Levy.

VII. GROUPING OF CLAIMS

With regard to the grounds of rejection related to issues I and II, claims 1-20 stand or fall together. Claim 1 is the representative claim for groups I and II.

VIII. ARGUMENTS

A. Levy Fails to Anticipate Claim 1 Under 35 U.S.C. § 102(b) By Failing to Disclose Each and Every Limitation of Claim 1

Appellant respectfully disagrees with the Examiner's rejection of claims 1-20 under 35 U.S.C. § 102(b) with respect to Levy. In particular, the Examiner has stated that:

> Regarding claims 1 and 17-20, Levy shows the claimed system memory controller as memory management unit 22 in Fig. 1, coupled to

memory bus 40. This system memory controller handles reads and writes as claimed.

Levy shows the claimed memory module as memory module 30 in Fig. 1. Memory module 30 includes the claimed plurality of memory devices as low stack 0-3 and high stack 0-3. Furthermore, memory module 30 includes the claimed memory module controller as memory transceiver 41 and memory control and timing unit 42. This controller receives a first memory transaction in a first format from the system memory controller and converts it into a second memory transaction in a second format for the plurality of memory devices as claimed. The second memory transaction is clearly different from the first memory format since the outputs of memory transceiver 41 and memory control and timing unit 42 are clearly different from their inputs. This is indicated by the differing nature of the signal lines shown in Fig. 1 and by the other figures and disclosure.

(pp.2-3 Final Office Action 8/8/00).

Appellant respectfully submits that claim 1 is not anticipated by Levy. To anticipate claim 1, Levy must disclose each and every limitation of claim 1. Claim 1 includes the limitations of:

> A system comprising:
> a system memory controller; and
> a first memory module comprising:
> a first plurality of memory devices;
> a first memory module controller coupled to the system memory controller and the first plurality of memory devices, the first memory module controller to receive from the system memory controller a first memory transaction in a first format and to convert the first memory transaction into a second memory transaction in a second format for the first plurality of memory devices, the second format of the second memory transaction being different from the first format of the first memory transaction.

(Claim 1)(emphasis added).

Levy, however, fails to disclose a first memory module controller coupled to the system memory controller and the first plurality of memory devices, the first memory module controller to receive from the system memory controller a first memory transaction in a first format and to convert the first memory transaction into a second memory transaction in a second format for the first plurality of memory devices as recited in claim 1. Levy further fails to disclose that the second format of the second memory transaction is different form the first format of the first memory transaction as recited in claim 1.

Levy, in Figure 1, discloses a memory module 30 coupled to associative memory 24. Memory module 30 includes a memory transceiver 41 and memory control and timing circuit 42 coupled to low and high stacks 44 and 45, respectively. The Examiner associates memory transceiver 41 and memory control and timing circuit 42 of Levy with the claimed first memory module controller as recited in claim 1.

The memory transceiver 41 and memory control and timing 42, however, are not related to converting or reformatting a memory transaction in a first format into a memory transaction in a second format. In particular, Levy discloses that:

> . . . During a writing operation, the associative memory 24 transmits BYTE MASK signals (FIG. 5) to the memory control and timing circuit 42 thereby to select one byte or some combination of bytes in the addressed location.
>
> Still referring to FIGS. 1 and 5, the associative memory 24 transmits an ADDRESS PARITY signal which is based upon the value of the address and various control signals that initiate a memory cycle and also data signals if data is being transferred from the associative memory 24. Next the associative memory 24 transmits a START signal that enables the memory control and timing circuit 42 (FIG. 1) to initiate a

> memory cycle. The circuit 42 transmits back to the associative memory 24 an ACKNOWLEDGE signal that terminates the address and control signals and the BYTE MASK, parity, data and START signals. During a reading memory cycle, the associative memory 24 can initiate another memory cycle with another memory until after the ACKNOWLEDGE signal is terminated.

(Levy Col. 8, lines 41-60).

Thus, Levy teaches that memory control and timing circuit 42 initiates a memory cycle after receiving BYTE MASK and ADDRESS PARITY signals. As such, the memory and control timing circuit of 42 of Levy does not teach converting a first memory transaction into a second memory transaction as recited in claim 1. Furthermore, nowhere in Levy does it disclose converting a first memory transaction into a second memory transaction and that the second memory transaction is different that the first memory transaction as recited in claim 1.

Therefore, for the above reasons, claim 1 is not anticipated by Levy under 35 U.S.C. 102(b) and is patentable over Levy because Levy does not disclose each and every limitation of claim 1.

A. Claim 1 is Patentable Over Levy Under 35 U.S.C. § 103(a) Because Levy Does not Disclose or Suggest Each and Every Limitation of Claim 1

Appellant respectfully submits that claim 1 is not obvious under 35 U.S.C. § 103(a) over Levy. For claim 1 to be rendered obvious by Levy, Levy must disclose or suggest each and every limitation of claim. Furthermore, the Examiner cannot rely on impermissible hindsight of the Appellant's disclosure.

In contrast to claim 1, Levy fails to disclose or suggest a first memory module controller coupled to the system memory controller and the first plurality of memory devices, the first memory module controller to receive from the system memory controller a first memory transaction in a first format and to convert the first memory transaction into a second memory transaction in a second format for the first plurality of memory devices as recited in claim 1.

In further contrast to claim 1, Levy fails to disclose or suggest the second format of the second memory transaction is different form the first format of the first memory transaction as recited in claim 1.

Levy discloses a memory control and timing circuit 42 to initiate a memory cycle. Nowhere in Levy does it disclose or suggest the memory control and timing circuit 42 to convert a first memory transaction into a second memory transaction and that the second memory transaction is different that the first memory transaction as recited in claim 1.

Therefore, claim 1 is patentable over Levy under 35 U.S.C. §103(a) because Levy does not disclose or suggest each and every limitation of claim 1.

Reviewing the claimed structure set forth in claims 1-20, the distinctions between the cited prior art and the claimed invention are readily apparent. Therefore, Appellant respectfully contends that once the Board reevaluates the applicability of the cited prior art in view of the limitations of the claims, it will be determined that the claims are clearly distinguishable over the prior art of record.

FEE FOR FILING A NOTICE OF APPEAL

Enclosed is a check in the amount of $300.00 to cover the fee for filing a Notice of Appeal required under 37 C.F.R. 1.1.7(e).

CHARGE OUR DEPOSIT ACCOUNT

If there are any further charges not accounted for herein, please charge them to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: Dec. 19, 2000

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APPENDIX

The claims on appeal read as follows:

1. A system comprising:

a system memory controller; and

a first memory module comprising:

a first plurality of memory devices;

a first memory module controller coupled to the system memory controller and the first plurality of memory devices, the first memory module controller ~~being configured~~ to receive from the system memory controller a first memory transaction in a first format and to convert the first memory transaction into a second memory transaction in a second format for the first plurality of memory devices, the second format of the second memory transaction being different from the first format of the first memory transaction.

2. The system of claim 1, further comprising:

a first memory bus coupled between the system memory controller and the first memory module controller.

3. The system of claim 2, wherein the first memory bus comprises a signal line for a clock signal.

4. The system of claim 2, wherein the first memory bus comprises:

a signal line for a handshake signal that indicates if the first memory module controller is communicating data to the system memory controller.

5. The system of claim 2, further comprising:

a second memory bus coupled between the first memory module controller and the first plurality of memory devices.

6. The system of claim 5, wherein the second memory bus comprises:

a signal line for a clock signal.

7. The system of claim 5, wherein the first memory bus is to operate at a first data rate and the second memory bus is to operate at a second data rate, and wherein the first data rate is different than the second data rate.

8. The system of claim 5, wherein the first memory bus has a first number of signal lines and the second memory bus has a second number of signal lines, and wherein the first number of signal lines is different than the second number of signal lines.

9. The system of claim 5, wherein the first memory module controller comprises:

request handling circuitry to receive the first memory transaction from the first memory bus; and

control logic coupled to the request handling circuitry and to reformat the first memory transaction into the second memory transaction on the second memory bus.

10. The system of claim 2, wherein the first memory bus is to carry time-multiplexed data and address information, and wherein the second memory bus includes separate address and data lines.

11. The system of claim 1, wherein the first memory module is a dual in-line first memory module (DIMM).

12. The system of claim 1, wherein the first memory module is a single in-line first memory module (SIMM).

13. The system of claim 1, wherein the first plurality of memory devices comprise volatile memory devices.

14. The system of claim 1, wherein the first plurality of memory devices comprise nonvolatile memory devices.

15. The system of claim 1, further comprising a second memory module including:

a second plurality of memory devices;

a second memory module controller coupled to the system memory controller and the second plurality of memory devices, the second memory module controller is to receive from the system memory controller a third memory transaction in the first format and is to convert the third memory transaction into a fourth memory transaction in the second format for the second plurality of memory devices, the second format of the fourth memory transaction being different from the first format of the third memory transaction.

16. The system of claim 15, wherein the first plurality of memory devices are to store data in a different way than the second plurality of memory devices.

17. A system comprising:

a system memory controller;

a memory bus coupled to the system memory controller; and

a memory unit including:

a plurality of memory devices, and

a memory module controller coupled to the memory bus and the plurality of memory devices, the memory module controller is to receive a first memory transaction from the memory bus in a first format and is to convert the first memory transaction into a second

memory transaction in a second format to at least one of the plurality of memory devices, the second format of the second memory transaction being different from the first format of the first memory transaction.

18. A method of communicating a memory transaction between a system memory controller and at least one of a plurality of memory devices on a memory module including a memory module controller, the method comprising:

sending a first memory transaction from the system memory controller to the memory module controller, the first memory transaction having a first format;

reformatting the first memory transaction into a second memory transaction for at least one of the memory devices, the second memory transaction having a second format that is different from the first format; and

sending the second memory transaction to the at least one of the memory devices.

19. The method of claim 18, wherein the memory transaction is a read transaction.

20. The method of claim 18, wherein the memory transaction is a write transaction.